L-Band Internally Matched Si-MMIC Front-End

Noriharu Suematsu, *Member, IEEE*, Masayoshi Ono, Shunji Kubo,
Yoshitada Iyama, *Member, IEEE*, and Osami Ishida, *Member, IEEE*

***Abstract*—A 1.9 GHz-band internally matched Si-MMIC front-end, fabricated in standard 0.8 μm BiCMOS process, was developed. This IC front-end contains a MOSFET T/R switch, a two-stage BJT low noise amplifier (LNA), and a down converter BJT mixer. Since the circuits are monolithically integrated on a low resistivity Si substrate, the coplanar waveguide (CPW) type spiral inductors are used to reduce the dielectric loss of on-chip matching circuits. The T/R switch has measured insertion loss of 2.5 dB and isolation of 25.5 dB at 0/3 V control voltage. The two-stage LNA has gain of 17.1 dB and noise figure (NF) of 2.9 dB at 2 V, 4 mA dc supply. The mixer has conversion gain of 5.9 dB and NF of 15 dB at 2 V, 1.7 mA dc supply. The measured performance of the fabricated Si-MMIC front-end indicates the possibility of application to mobile communication handset terminals.**

I. Introduction

In RECENT years, there is an increasing demand for low production cost RF IC front-end used in handset terminals for mobile communication [1]–[4]. The Si-IC fabricated in BiCMOS process [3]–[5] is one of those developed for such applications. Since the standard BiCMOS process [6]–[7] uses relatively low resistivity Si substrate (about 10 Ω cm), the loss of on-chip matching circuits, especially that of spiral inductor, is quite high, due to the dielectric loss of Si substrate in the microwave frequency range [7]–[9]. For this reason, most of Si-IC's have used spiral inductors only as bias circuits, and have needed external matching circuits [3]–[5]. Some modifications of BiCMOS process have been tried to reduce the dielectric loss by using high resistivity (several kΩ cm) Si substrate [10], or by using thick polyimide (10 μm thickness) as insulator [8]. In this paper, the CPW type spiral inductor is described, which offers superior feature in comparison with microstrip (MS) type spiral inductor. By selecting CPW type spiral inductor for matching circuits, it is possible to reduce the insertion loss which comes from the dielectric loss of the low resistivity Si substrate. The configuration and the measured performance of the fabricated L-band Si-MMIC front-end with CPW type on-chip matching circuits are also described. This IC front-end contains an enhancement mode N-type MOSFET T/R switch [11], a two-stage bipolar junction transistor (BJT) LNA and a BJT mixer. The CPW type spiral inductors are used in the input and output matching circuits of the LNA and RF input and LO input matching circuits of the mixer.

Manuscript received March 29, 1996.

N. Suematsu, M. Ono, Y. Iyama, and O. Ishida are with the Information Technology R&D Center, Mitsubishi Electric Corporation, Kamakura City, Kanagawa 247, Japan (e-mail: suematsu@micro4.isl.melco.co.jp).

S. Kubo is with the ULSI Laboratory, Mitsubishi Electric Corp., Itami City, Hyogo 664, Japan.

Publisher Item Identifier S 0018-9480(96)08531-6.

TABLE I
EXTRACTED EQUIVALENT CIRCUITS PARAMETERS AND THE ATTENUATION OF CPW AND MS TYPE FOUR-TURN SPIRAL INDUCTORS. (OUTER SIZE: 300 μm$\times$ 300 μm, CONDUCTOR THICKNESS. 3.5 μm, STRIPLINE WIDTH. 11 μm, LINE SPACE: 10 μm)

Type	CPW	MS
L_s	4.2	4.2
C_p	0.4	0.46
R_s (Ω)	4.6	3.3
R_p (Ω)	136	2.46
Attenuation (dB)	1.5	1.8

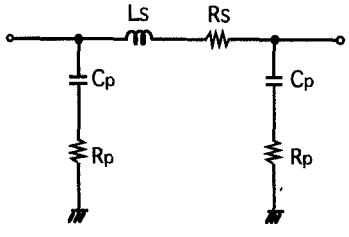


Fig. 1. Equivalent circuit of spiral inductor fabricated on low resistivity Si substrate. R_s represents the conductor loss, R_p represents the dielectric loss of the spiral inductor, L_s represents the inductance component of the spiral inductor, and C_p represents the stripline-substrate capacitance.

II. Features of CPW Type Spiral Inductor

The loss of spiral inductors is dominant among the losses of the internal matching circuits for L-band LNA and mixer used in RF front-end. In order to reduce the conductor loss, the stripline thickness of 3.5 μm is achieved by stacking second, third and fourth aluminum conductor layer. Then the reduction of dielectric losses of low resistivity Si substrate is desirable. Equivalent circuit parameters and attenuation are compared between CPW and MS type spiral inductor. The equivalent circuits of spiral inductor fabricated on a low resistivity Si substrate is shown in Fig. 1. Series resistance R_s represents the conductor loss and parallel resistance, R_p represents the dielectric loss of the spiral inductor, L_s represents the inductance component of the spiral inductor, and C_p represents the stripline-substrate capacitance. Table I shows the extracted equivalent circuits parameters and the attenuation of CPW and MS type four-turn spiral inductors having 300 μm$\times$ 300 μm outer size, 3.5 μm aluminum conductor thickness, 11 μm stripline width and 10 μm line space. The resistivity of Si substrate is about 10 Ωcm, and the insulator between aluminum stripline and Si substrate is 1 μm thick SiO_2 layer. In the case of the CPW, R_s is 40% higher and R_p is 45% lower than that in the case of the MS. In this case, the CPW type spiral inductor has 22% lower attenuation than MS type spiral inductor has, because of the lower R_p, that is, lower dielectric loss.

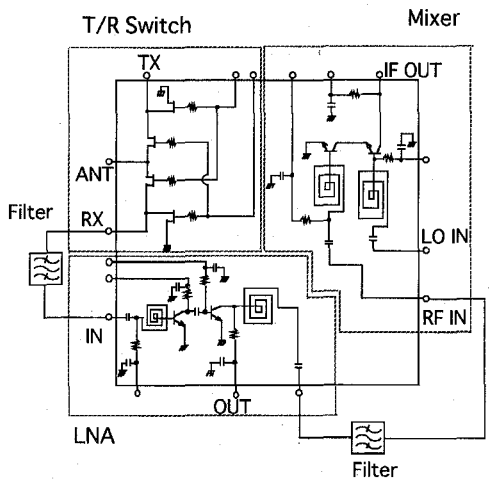


Fig. 2. Schematic diagram of Si-MMIC front-end.

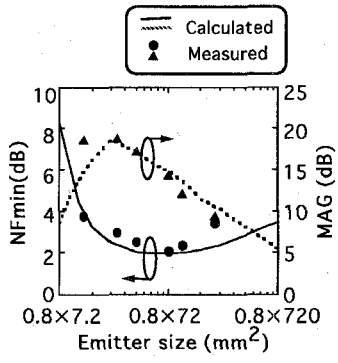


Fig. 3. Emitter size dependence of BJT's NF_{min} and MAG measured at 1.9 GHz. The bias condition is $V_{ce} = 1.2$ V, $I_{ce} = 2$ mA. The calculated data derived from extracted SPICE parameters. The lowest NF_{min} of 1.9 dB and MAG of 14.5 dB are achieved at emitter size of 0.8 μm × 72 μm.

III. Configuration of IC Front-End

The schematic diagram of Si-MMIC front-end is shown in Fig. 2. This IC consists of a MOSFET T/R switch, a two-stage BJT low noise amplifier (LNA), and a down converter BJT mixer. External filters can be connected between RX port of T/R switch and IN port of LNA and between OUT port of LNA and RF IN port of mixer. In order to obtain higher isolation, all bias circuits are separated among T/R switch, LNA, and mixer.

A. T/R Switch

Enhancement mode N type MOSFET's (gate length $(L_g) = 0.8$ μm, gate width $(W_g) = 400$ μm, both are in mask size) are used as switching elements, and are switched by gate control voltage of 0 V (OFF state)/3 V (ON state). All control bias ports are connected to FET gate through 2 kΩ resistors. In order to achieve higher isolation in OFF state, the FET's are series-shunt connected.

B. LNA

There is an optimum emitter size to achieve the lowest NF_{min} under the constant dc supply current and voltage. In the case of smaller emitter size, the NF_{min} increases with increasing base resistance. On the other hand, in the case of larger emitter size, the NF_{min} increases with decreasing current density per unit emitter size. The emitter size dependence of the BJT's NF_{min} and maximum available gain (MAG) measured at 1.9 GHz is shown in Fig. 3. The calculated data derived from extracted SPICE parameters. With 1.2 V and 2 mA dc supply, the lowest NF_{min} of 1.9 dB and MAG of 14.5 dB are achieved at emitter size of 0.8 μm × 72 μm (mask size). Then the emitter size of BJT for LNA is designed as 0.8 μm × 72 μm. The input port is NF matched, and the output port is gain matched to 50 Ω internally, by using CPW type spiral inductors. The collectors of the BJT's are biased through 400 Ω resistor. The collector-emitter voltage of both BJT's is 1.2 V at supplied dc current of 2 mA each and voltage of 2 V.

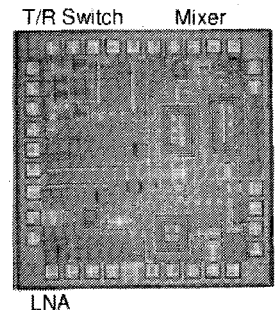


Fig. 4. Photograph of fabricated Si-MMIC front-end with internal matching spiral inductors. The chip size is 2 mm × 2 mm.

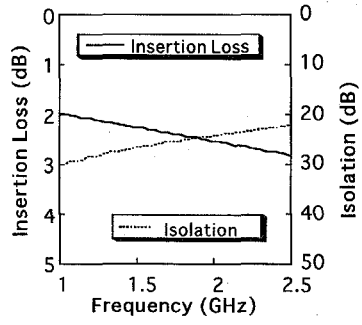


Fig. 5. Small signal characteristics of T/R MOSFET switch. The control voltage is 0 V (off state) and 3 V (on state). The insertion loss is 2.5 dB and the isolation is 25.5 dB at 1.9 GHz.

C. Mixer

Two BJT's, having same emitter size as those used in LNA, are connected in series. RF and LO signals are introduced to the base of BJT's separately. RF and LO ports are internally matched by using CPW type spiral inductors and resistor. The collector is biased through 400 Ω resistor which is connected to IF output. IF port requires external matching circuits.

IV. Measured Results

A photograph of fabricated Si-MMIC front-end with internal matching spiral inductors is shown in Fig. 4. The chip size is

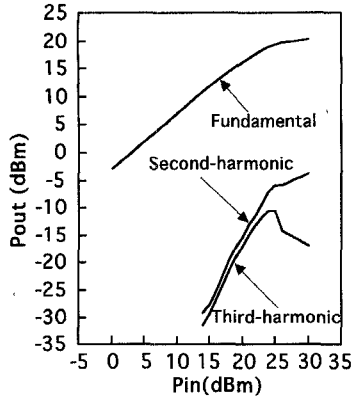


Fig. 6. Transfer characteristics of T/R MOSFET switch measured at 1.9 GHz. The control voltage is 0 V (off state) and 3 V (on state). The insertion loss degradation begins at input power of 23 dBm.

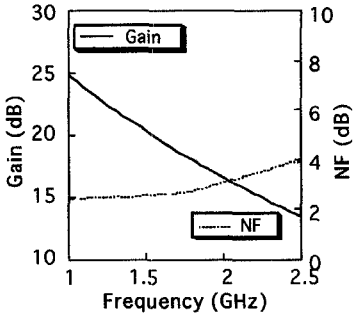


Fig. 7. Frequency dependence of gain and NF of two-stage BJT LNA. The bias condition is $V_{cc} = 2$ V, $I_{ce} = 4$ mA (2 mA for each BJT). The gain is 17.1 dB and the NF is 2.9 dB at 1.9 GHz.

2 mm × 2 mm, and the IC is fabricated in standard 0.8 μm BiCMOS process [6]. All spiral inductors consist of 3.5 μm thick and 11 μm wide aluminum stripline.

The small signal characteristics of T/R switch is shown in Fig. 5. The insertion loss is 2.5 dB and the isolation is 25.5 dB at 1.9 GHz. The transfer characteristics of T/R switch measured at 1.9 GHz is shown in Fig. 6. The insertion loss degradation begins at input power of 23 dBm. Up to 30 dBm, the FET destruction can not be observed. In order to improve the insertion loss and the saturated power, adopting lower threshold voltage FET or/and silicided source-drain structure FET will be a candidate.

The frequency dependence of gain and NF of two-stage BJT LNA is shown in Fig. 7. The loss of dc cut capacitors at input and output ports is excluded. The bias condition is $V_{cc} = 2$ V, $I_{ce} = 4$ mA (2 mA for each BJT). The gain is 17.1 dB and the NF is 2.9 dB at 1.9 GHz. The frequency dependence of return loss of the LNA is shown in Fig. 8. Since the input port is NF matched, the input return loss is 7.0 dB, but the output return loss is 16.6 dB at 1.9 GHz. Both ports are matched in a wide band, because of the relatively low Q spiral inductor.

The frequency dependence of conversion gain and NF of BJT mixer is shown in Fig. 9. This performance excludes the loss of dc cut capacitor at both RF and LO input ports. The bias condition is $V_{cc} = 2$ V, $I_{ce} = 1.7$ mA, and LO power is

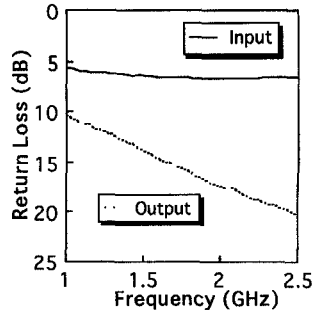


Fig. 8. Frequency dependence of return loss of two-stage BJT LNA. The bias condition is $V_{cc} = 2$ V, $I_{ce} = 4$ mA (2 mA for each BJT). The input return loss is 7.0 dB and the output return loss is 16.6 dB at 1.9 GHz.

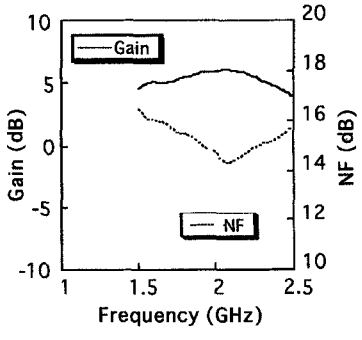


Fig. 9. Frequency dependence of conversion gain and NF of BJT mixer. The bias condition is $V_{cc} = 2$ V, $I_{ce} = 1.7$ mA, IF frequency is 240 MHz, and LO power is 0 dBm. The conversion gain is 5.9 dB and the NF is 15 dB at 1.9 GHz RF frequency.

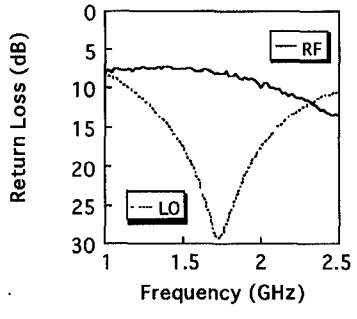


Fig. 10. Frequency dependence of RF and LO return loss of BJT mixer measured at 0 dBm LO power. The bias condition is $V_{cc} = 2$ V, $I_{ce} = 1.7$ mA. When RF frequency is 1.9 GHz and LO frequency is 1.66 GHz, the return loss is 8.0 dB at RF input port and 21 dB at LO input port.

0 dBm. The conversion gain is 5.9 dB and the NF is 15 dB at 1.9 GHz RF frequency. The frequency dependence of RF and LO return loss of the mixer measured at 0 dBm LO power is shown in Fig. 10. When RF frequency is 1.9 GHz and LO frequency is 1.66 GHz, the return loss is 8.0 dB at RF input port and 21 dB at LO input port. The LO power dependence of conversion gain and NF of the mixer is shown in Fig. 11. RF frequency is 1.9 GHz, and IF frequency is 240 MHz. Below −10 dBm LO power, the conversion gain rapidly decreases, and the NF rapidly increases.

By using this IC, the RF front-end having NF of 6.6 dB, including T/R switch, can be realized at 1.9 GHz with 11.4 mW dc power consumption.

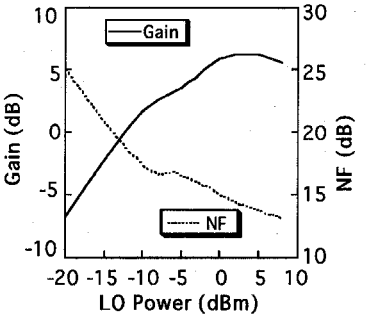


Fig. 11. LO power dependence of conversion gain and NF of BJT mixer. The RF frequency is 1.9 GHz, and IF frequency is 240 MHz. The bias condition is $V_{cc} = 2$ V, $I_{ce} = 1.7$ mA. Below -10 dBm LO power, the conversion gain rapidly decreases, and the NF rapidly increases.

V. Conclusion

An L-band Si-MMIC front-end with fully monolithic internal matching circuits was developed. This IC is fabricated on a low resistivity Si substrate in standard 0.8 μm BiCMOS process. It contains a T/R switch, a two-stage LNA and a down converter mixer. By using CPW type spiral inductors, on-chip matching circuits with lower insertion loss can be achieved. The performance of this IC front-end at 1.9 GHz with low dc power consumption shows the possibility of application to mobile handset terminals.

References

[1] Y. Imai, M. Tokumitsu, and A. Minakawa, "Design and performance of low-current GaAs MMIC's for L-band front-end applications," *IEEE Trans. Microwave Theory Tech.*, vol. 39, no. 2, pp. 209–215, 1991.

[2] N. Suematsu, M. Shimozawa, K. Mori, Y. Nakajima, K. Maemura, and O. Ishida, "Low power consumption RF IC's for Japanese mobile handset terminals," in *Proc. 1995 IEEE Int. Topical Meet. Nomadic Microwave Tech. and Tech. for Mobile Commun. Detection*, 1995, pp. 39–42.

[3] K. O. P. Garone, C. Tsai, G. Dawe, B. Scharf, T. Tewksbury, C. Kermarrec, and J. Yasaitis, "A low cost and low power silicon *npn* bipolar process with NMOS transistors (ADRF) for RF and microwave applications," *IEEE Trans. Electron Devices*, vol. 42, pp. 1831–1840, Oct. 1995.

[4] S. Lee and R. D. Schultz, "Production DC screening for RF performance of a 900 MHz monolithic low noise amplifier," in *Proc. IEEE 1995 Microwave Millimeter-Wave Monolithic Circ. Symp.*, 1995, pp. 69–72.

[5] J. R. Long, M. A. Copeland, P. Schvan, and R. A. Hadaway, "A low-voltage silicon bipolar RF front-end for PCN receiver application," in *Proc. 1995 IEEE ISSCC Dig. Tech. Papers*, 1995, pp. 140–141.

[6] T. Ikeda, T. Nakashi, S. Kubo, H. Jouba, and M. Yamawaki, "A high performance BiCMOS with novel self-aligned vertical *PNP* transistors," in *Proc. IEEE 1994 Bipolar/BiCMOS Circ. Technol. Meet.*, 1994, pp. 238–241.

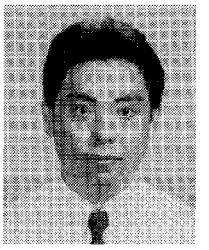
[7] D. Lovelace, N. Camilleri, and G. Kannell, "Silicon MMIC inductor modeling for high volume, low cost applications," *Microwave J.*, pp. 60–71, Aug. 1994.

[8] B. Kim, B. Ko, K. Lee, J. Jeong, K. Lee, and S. Kim, "Monolithic planar RF inductor and waveguide structures on silicon with performance comparable to those in GaAs MMIC," in *Proc. IEDM-95*, 1995, pp. 717–720.

[9] J. N. Burghartz, M. Soyuer, and K. A. Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Trans. Microwave Theory Tech.*, vol. 44, no. 1, pp. 100–104, 1996.

[10] A. C. Reyes, S. M. El-Ghazaly, S. J. Dorn, M. Dydyk, D. K. Schroder, and H. Patterson, "Coplanar waveguides and microwave inductors on silicon substrates," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 9, pp. 2016–2022, 1995.

[11] Y. Iyama, N. Suematsu, T. Shigematsu, T. Moriwaki, and T. Ikeda, "L-band SPDT switch using Si-MOSFET," *IEICE Trans. Electron.*, vol. E79-C, no. 5, pp. 636–643, 1995.



Noriharu Suematsu (M'92) received the B.S. and M.S. degrees in electronics and communication engineering from Waseda University, Tokyo, Japan, in 1985 and 1987, respectively.

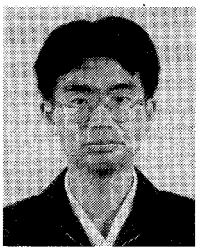
In 1987, he joined Mitsubishi Electric Corporation, where he has been engaged in research and development of microwave and millimeter-wave solid state circuits. During 1992–1993, he was a Visiting Researcher at the University of Leeds, United Kingdom.

Mr. Suematsu is a member of the Institute of Electronics, Information and Communication Engineers of Japan (IEICE) and the Japan Society of Applied Physics. In 1991, he received the Shinohara Award from the IEICE.

Masayoshi Ono received the B.S. and M.S. degrees in electrical and communication engineering from Tohoku University, Sendai, Japan, in 1992 and 1994, respectively.

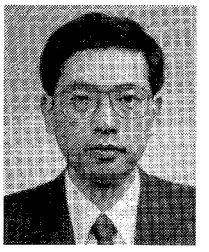
In 1994, he joined Mitsubishi Electric Corporation, where he has been engaged in research and development of MMIC's for wireless applications.

Mr. Ono is a member of IEICE.



Shunji Kubo received the B.S. and M.S. degrees in chemistry from Kobe University, Hyogo, Japan, in 1990 and 1992, respectively.

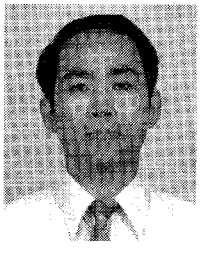
In 1992, he joined Mitsubishi Electric Corporation, where he has been engaged in research and development of bipolar and BiCMOS process technology.



Yoshitada Iyama (M'94) received the B.S. and M.S. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1978 and 1980, respectively.

In 1980, he joined Mitsubishi Electric Corporation, where he has been engaged in research and development of microwave control circuits and monolithic microwave IC's.

Mr. Iyama is a member of IEICE.



Osami Ishida (M'89–SM'95) received the B.S. and M.S. degrees in electronic engineering, and Dr.Eng. degree from the Shizuoka University, Hamamatsu, Japan, in 1971, 1973, and 1992, respectively.

In 1973, he joined Mitsubishi Electric Corporation. He has been a Manager in the Aperture Antenna Group from 1988 to 1992, Deputy Manager in the Opto and Microwave Electronics Department from 1993 to 1995, and is presently a Manager in the Microwave Electronics Department at the Information Technology R&D Center. He has been engaged in research and development of microwave circuit technologies in antenna feeds for satellite communication and phased array radars, and in devices for mobile communication.

Dr. Ishida is a member of IEICE, and served as a member of the Editorial Committee for the *Transactions of IEICE* from 1988 to 1992.